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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/716,808	CELELLA ET AL.
	Examiner	Art Unit
	John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-14* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1204//27 Dec 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 4 is objected to because of the following informalities:

In Claim 4, "said increased conductivity" has no antecedent basis. This objection can be easily overcome by changing the dependency from claim 2 to claim 3. Accordingly, in line 1 of Claim 4, "2" should be changed to --3--.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections below:

Weatherley (US 6,333,472 B1) Winings (US 6,250,968 B1)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-4, 6-8 and 10-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Weatherley.

As to Claim 1, Weatherley discloses a printed circuit board 1 comprising: first plated through-holes 2 for receiving a first connecting component (Fig. 1; col.3: 54-59); second plated through-holes 3 for receiving a second connecting component (Fig. 1; col.3: 60-63); a signal carrying trace 5 for transmitting a signal from one of the first plated through-holes 2 (marked t1 in Fig. 3-1) to one of the second plated through-holes 3 (marked T1 in Fig. 3-1; col.4: 30-35); a trace 6 (inherently, trace 6 is a phase delay control trace) in electrical connection with plated through-hole t1, the phase delay control trace 6 inherently affecting delay of the signal from first plated through-hole t1 to second plated through hole T1 (Fig. 3-1; col.3: 26-30 and col.4: 30-36). *Examiner's Note*: While Weatherley does not explain how the "loop" configurations--that branch from a single track (5, for example, in Fig. 3-1) into two tracks 6 then converge back into a single track 5--perform the crosstalk reduction, the Weatherley configuration nevertheless appears to be structurally and functionally the same as that in Applicant's disclosure (see disclosure Fig. 6 and Specification, p.6, paragraph [0026]), wherein Weatherley's trace 6 (Fig. 3-1) functions as the "redundant" trace analogous to the redundant trace 60 in Applicant's Fig. 6 and therefore inherently performs the same

phase delay control function as does Applicant's redundant trace 60 for reducing crosstalk.

As to Claim 2, Weatherley further discloses phase delay control trace 6 is the same as the signal carrying trace 5 (i.e., trace 6 is a structural part of signal trace 5; col.3: 26-30 and col.4: 35-36).

As to Claim 3, Weatherley discloses that the signal trace 5 separates into redundant traces 6, thus, inherently, providing less resistance between (i.e., increased conductivity) between first plated through-hole t1 and second plated through-hole T1, and thereby affecting the phase delay of the signal from first plated through-hole t1 to second plated through-hole T1 (Fig. 3-1; col.3: 26-30 and col.4: 35-36). *Examiner's Note*: again, as in Claim 1, Weatherley does not explicitly point out the particular affect on the signal of the branched ("loop") signal line structure that effects the crosstalk compensation, but the structure nevertheless appears to be the same as the signal line structure taught in Fig. 6 and paragraph [0026] of the Applicant's disclosure and therefore, inherently, the two-track branch of the phase control trace 6 affects the phase delay of the signal from hole t1 to T1, as in the Applicant's signal line structure.

As to Claim 4, Weatherley further discloses the phase delay control trace includes multiple--in the case of signal trace 5, the control trace 6 includes two--redundant phase delay control traces (signal trace 5 branches into two control traces 6, as shown in Fig. 3-1) in order to provide the increased conductivity.

As to Claim 6, Weatherley further discloses the phase delay control trace 8 (also in Fig. 3-1) is an isolated dead end trace--the "dead end" being the end of the loop on

the obverse surface of the board in Fig. 3-1--separate from signal carrying trace 5, the dead end trace 8 inherently avoiding reactive coupling with the other traces due to its isolation (Fig. 3-1; col.3: 30-35 and col.4: 38-41).

As to Claim 7, Weatherley further discloses the phase delay control trace includes a first phase delay control trace 6 and a second phase delay control trace 8 (Fig. 3-1; col.4: 35-36 and 38-41).

As to Claim 8, Weatherley further discloses the first phase delay control trace 6 is the same as the signal carrying trace 5 (col.4: 35-36); and the second phase delay control trace 8 is an isolated dead end trace separate from signal carrying trace 5, the dead end trace 8 inherently avoiding reactive coupling with the other traces due to its isolation (Fig. 3-1; col.3: 30-35 and col.4: 38-41).

As to Claim 10, Weatherley further discloses the first phase delay control trace 6 includes multiple (i.e., two branched) redundant phase delay control traces 6 (Fig. 3-1) in order to affect the phase delay of the signal from first plated through-hole t1 to second plated through-hole T1 (Fig. 3-1). *Examiner's Note*: again, as in Claim 1, Weatherley does not explicitly point out the particular affect on the signal of the branched ("loop") signal line structure that effects the crosstalk compensation, but the structure nevertheless appears to be the same as the signal line structure taught in Fig. 6 and paragraph [0026] of the Applicant's disclosure and therefore, inherently, the two-track branch of the phase control trace 6 affects the phase delay of the signal from hole t1 to T1, as in the Applicant's signal line structure.

As to Claim 11, Weatherley further discloses the first connecting component is an outlet (col.3: 54-59).

As to Claim 12, Weatherley further discloses the second connecting component is a wire termination block (col.3: 60-65).

As to Claim 13, Weatherley further discloses a crosstalk magnitude control trace (Fig. 3-7; the curved trace that connects to the ends of trace 33) in electrical connection with one of the first plated through-holes t1-7--in particular, t7--, the crosstalk magnitude trace being reactively coupled with another trace (i.e., trace 33) along a portion of signal line 33, inherently controlling crosstalk magnitude. *Examiner's Note*: as pointed out by the Applicant in paragraph [0025] of Applicant's disclosure, running traces adjacent to each other, as is done along a portion of the signal line 33 in Fig. 3-7 of Weatherley, "provides compensating crosstalk to counteract offending crosstalk."

As to Claim 14, Weatherley discloses: a first component for connection with a first cable (col.3: 54-59 and col.5: 30-42); a second component for connection with a second cable (col.3: 60-64 and col.5: 30-42); a printed circuit board 1 (Fig. 2) providing crosstalk compensation, the printed circuit board 1 including: first plated through-holes 2 for receiving a first connecting component (Fig. 1; col.3: 54-59); second plated through-holes 3 for receiving a second connecting component (Fig. 1; col.3: 60-63); a signal carrying trace 5 for transmitting a signal from one of the first plated through-holes 2 (marked t1 in Fig. 3-1) to one of the second plated through-holes 3 (marked T1 in Fig. 3-1; col.4: 30-35); a trace 6 (inherently, trace 6 is a phase delay control trace) in electrical connection with plated through-hole t1, the phase delay control trace (branched trace 6)

inherently affecting delay of the signal from first plated through-hole t1 to second plated through hole T1 (Fig. 3-1; col.3: 26-30 and col.4: 30-36). *Examiner's Note*: While Weatherley does not explain how the "loop" configurations--that branch from a single track (5, for example, in Fig. 3-1) into two tracks 6 then converge back into a single track 5--perform the crosstalk reduction, the Weatherley configuration nevertheless appears to be structurally and functionally the same as that in Applicant's disclosure (see disclosure Fig. 6 and Specification, p.6, paragraph [0026]), wherein Weatherley's trace 6 (Fig. 3-1) functions as the "redundant" trace analogous to the redundant trace 60 in Applicant's Fig. 6 and therefore inherently performs the same phase delay control function as does Applicant's redundant trace 60 for reducing crosstalk.

5. Claims 1-3, 5 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Winings.

As to Claim 1, Winings discloses a printed circuit board 301 (Figs. 4, 5, 6A,B; col.4: 56-58) comprising: first plated through-holes 311 for receiving a first connecting component and second plated through-holes 313 for receiving a second connecting component (col.4: 66-col.5: 5); a signal carrying trace C3,a for transmitting a signal from one of first plated through-holes 311 to one of second plated through-holes 313 (Fig. 6B; col.5: 57-64); a phase delay control trace (wide portions 323 and 327 of signal trace C3,a) in electrical connection with one of first plated through-holes 311, the phase delay control trace affecting phase delay of the signal from first plated through-hole 311 to second plated through-hole 313 (Fig. 6B; col.6: 27-43). *Examiner's Note*: Although Winings does not state that the wide portion (323, 327) of signal trace C3,a performs a

phase delay control function, the Examiner takes the position that it inherently performs a phase delay control function in view of the teaching provided in paragraph [0027] on p. 6 of Applicant's disclosure, wherein Applicant teaches that: "Additionally, phase delay may be altered by varying the trace width. For example [as shown in Fig. 7 of Applicant's disclosure], signal carrying trace 61 between through hole 41 and through hole 51 is thicker. This provides less resistance and thus less delay." Accordingly, the Examiner believes that the wide portion (323, 327) of signal trace C3,a inherently performs that exact same phase delay control function, by virtue of its wider (thicker) geometry in portion (323, 327).

As to Claim 2, Winings further discloses phase delay control trace (portion 323 and 327 of signal trace C3,a) is the same as the signal carrying trace C3,a (Fig. 6B; col.6: 27-29 and 34-43).

As to Claim 3, because the phase delay control trace C3,a of Winings includes the wide portion 323 and 327, it inherently has an increased conductivity; the increased conductivity affecting the phase delay of the signal from first plated through-hole 311 to second plated through-hole 313 (as implied in Winings, col.6: 34-43 and specifically taught as an inherent property of the similar signal trace configuration found in Fig. 7 and paragraph [0027] of Applicant's disclosure).

As to Claim 5, Winings further discloses the phase delay control trace includes increased dimensions (in portions 323, 327) in order to provide the increased conductivity (the wider trace portions 323, 327 inherently provide the increased conductivity).

As to Claim 13, Winings further discloses another layer of circuit board 301 (Fig. 14)--in addition to the layer 319 of Figs. 6A,B--wherein a crosstalk magnitude control trace C17,b in electrical connection with one of the first plated through-holes 511 (of circuit board layer 545), the crosstalk magnitude control trace being reactively coupled (at section A) with signal trace C14,a (Fig. 14; col.8: 56-61).

Allowable Subject Matter

6. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Curry et al. (US 6,379,157 B1) discloses a printed circuit board comprising multipoint compensative reactive coupling at different time delay distances from origination points of unwanted crosstalk (Abstract, col.17: 5-col.23: 52).

b) AbuGhazaleh et al. (US 6, 796,847 B2) discloses phase delay compensation by structuring the plug contacts accordingly (col.1: 48-57; col.6: 31-col.7: 6; col.7: 30-

49). Apparently, the circuit board 16 in Figs. 12 and 13 further reduces the crosstalk by reactive couplings in the wiring (col.5: 13-44; col.7: 30-49).

c) Ferry (US 6,096,980) discloses non-ohmic (i.e., "dead-end") traces that reduce crosstalk through the effects of capacitive and inductive coupling (col.3: 54-64 and col.4: 1-51).

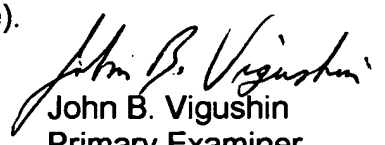
d) Gurovich et al. (US 2004/0248468 A1) discloses crosstalk-reducing stubs (i.e., "dead-end" traces) which create a compensation crosstalk that counteracts the offending crosstalk (Figs. 3A, 4A and 6; paragraphs [0050], [0070], [0073] and [0077]).

e) Adriaenssens et al. (US 5,997,358) discloses, in Fig. 10, a printed circuit board with crosstalk compensative wiring configurations along sections (stages) I, II and III that provide multiple stages of compensating crosstalk having magnitude and phase that substantially eliminate the offending near end crosstalk (col.9: 39-57).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
November 02, 2005